REMARKS:

Applicants have carefully studied the nonfinal Examiner's Action and all references cited therein. The amendment appearing above and these explanatory remarks are believed to be fully responsive to the Action. Accordingly, this important patent application is now believed to be in condition for allowance.

Specification

Applicants have amended the specification to correct the noted informalities. Applicants assert that no new matter has been introduced by the amendment.

Drawings

The specification has been amended to add the reference character "**110**", which was inadvertently omitted from the specification as originally filed. No new matter has been introduced by the amendment. Accordingly, the drawings are now believed to be in compliance with 37 CFR 1.84(p)(5) as required.

Claim Objections

Applicants have amended the claims to correct the noted informalities. Applicants assert that the claims, as amended, are now in condition for allowance.

Claim Rejections – 35 U.S.C. § 103

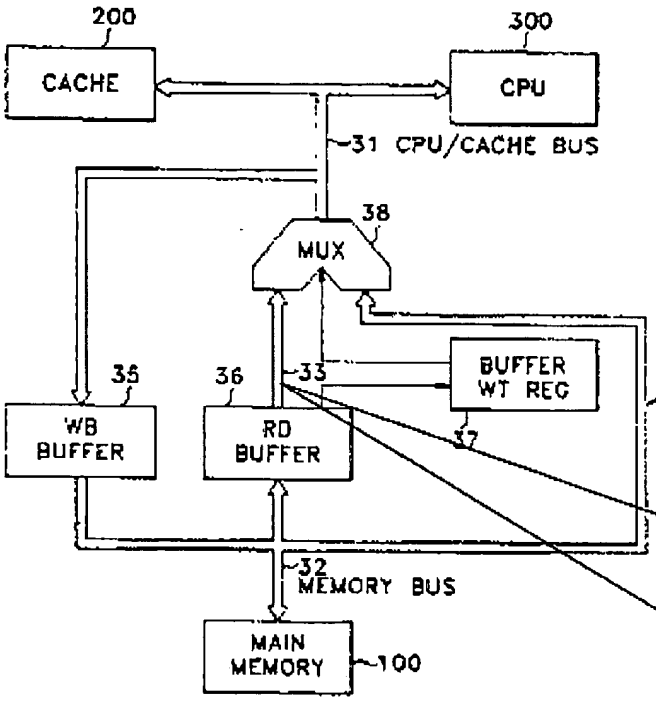
Applicants acknowledge the quotation of 35 U.S.C § 103(a).

Claims 1-24 stand rejected under 35 U.S.C § 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Park et al. [US 5,526,508 A; hereinafter Park].

Regarding independent claim 1, the Office states that Park discloses a method for a cache line replacing system wherein said method for reducing latency in information transfers to a bus includes transferring information to a bus if the buffer is empty and the transferring of information to the bus in allowed.

More specifically, the Office states that Park discloses transferring a line of cache data to a CPU/Cache bus if an RD Buffer is empty, as indicated by a Buffer WR Reg count of 'zero', at Fig. 3 and col. 5, lines 26-30, and transferring of the cache data to the bus is allowed, as is the case when the CPU/Cache bus in idle after write-back data has been stored in the write-back buffer as described at col. 3, lines 27-35 and col. 4, lines 31-46.

Applicants respectfully disagree with the finding of the Office. Park et al. describes in the Abstract and with reference to Fig. 3, a cache line replacing apparatus having a read buffer for storing data which is read from the main memory and a register for increasing the count value of the register when data is stored to the read buffer and decreasing the count value of the register when the data is read from the read buffer. The apparatus further includes a multiplexer for selectively transmitting the data stored in the read buffer to the CPU bus or transmitting the data directly from the memory bus to the CPU bus, thereby bypassing the buffer, according to the count value of the register. As such, in accordance with the teaching of Park, each time data is written to the read buffer, the count value of the register increases. Upon completion of the write-back cycle as described by Park, the multiplexer selects the output of the read buffer for transmission to the CPU bus. The data that was stored is the read buffer is then transmitted to the CPU bus and the count value of the register decreases until the buffer is empty and, accordingly, the count value of the register is zero. When the count value of the register is zero, no data exists in the read buffer and therefore the multiplexer deselects the read buffer output and selects the direct output from the memory bus to be transmitted to the CPU bus, therefore bypassing the read buffer.



When the count value of BUFFER WT REG is zero, data flows directly from the memory bus, through the MUX, to the CPU bus. Regardless of the CPU/cache bus availability.

When the count value of BUFFER WT REG is greater than zero, that is an indication that a write-back has occurred and that there is data available in the RD BUFFER. The MUX then selects to transfer the data from RD BUFFER to the CPU bus until the count value has been decreased to zero. Regardless of the CPU/cache bus availability.

The present invention describes and claims the steps of writing information to a buffer if a bus grant indication indicates that transfer of the information to the bus is not allowed. However, if the bus grant indication indicates that transferring of the information to the bus is allowed and the buffer is empty, then the information is transferred to the bus, thereby bypassing the buffer.

Park et al. does not describe the use of a bus grant indication to determine if the transfer of information to the bus is allowed. The Office states that Park describes transferring information to a bus if a buffer is empty and the transfer of the information to the bus is allowed. To support this statement, the Office states that Park describes the CPU/cache bus as being idle after the write-back data has been stored in the write-back buffer, at col. 3, lines 27-35, and col. 4, lines 31-46. Applicants respectfully disagree with the Office regarding this finding. Park does not describe the bus as being idle after the write-back process is completed. In fact, with reference col. 4, lines 31-36 of Park, the data stored in the read buffer **36** is stored during the time when the write-back data is being stored in the write-back buffer **35**. Then, immediately after the storage of the write-back data is completed, the data of the read buffer **35** is transmitted to the CPU/cache bus **31** through multiplexer **38**. As described by Park at col. 4, lines 45-47, the multiplexer **38** continuously transmits the data of memory bus **32** to the CPU/cache bus **31** when the value of register **37** becomes zero. Clearly, Park does not describe a step for the determination of whether or not the CPU/cache bus **31** is available for transfer, but rather that the data is continuously transmitted regardless of the status of the CPU/cache bus **31**. Additionally, Park does not employ a bus grant indication or any other form of indication as to whether or not the bus is available for transfer.

To establish a *prima facie* case of obviousness, the prior art must cited must teach or suggest all the claim limitations. Neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest the step of "transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed" as is recited in claim 1. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

Regarding independent claim 9, the Office states that Park discloses logic configured to cause information to be transferred from the device to the bus if the buffer is empty and transfer of the information to the bus is allowed. The Office cites the MUX 38 and Buffer WT Reg 37 of Fig. 3 in support of this statement. Additionally, the Office states that the CPU/Cache bus is idle after the write-back data is stored in the write-back buffer and as such, the transfer of the information to the bus is allowed.

Applicants respectfully disagree with the finding of the Office. Park does not describe logic configured to cause information to be transferred from the device to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed. As previously described, Park teaches at col. 4, lines 45-47, that the multiplexer 38 continuously transmits the data of memory bus 32 to the CPU/cache bus 31 when the value of register 37 becomes zero. Clearly, Park does not describe logic configured to cause information to be transferred from the device "to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed," as is recited in claim 9. Rather, Park describes the data as being continuously transmitted regardless of the status of the CPU/cache bus 31.

To establish a *prima facie* case of obviousness, the prior art must cited must teach or suggest all the claim limitations. Neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest logic configured to cause information to be transferred from the device to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

Regarding independent claim 19, the Office states that Park discloses logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus. The Office cites the MUX 38 and Buffer WT Reg 37 of Fig. 3 in support of this statement. Additionally, the Office states that the CPU/Cache bus is idle after the write-

back data is stored in the write-back buffer and as such, the transfer of the information to the bus is allowed.

Applicants respectfully disagree with the finding of the Office. Park does not describe logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus. As previously described, Park teaches at col. 4, lines 45-47, that the multiplexer **38** continuously transmits the data of memory bus **32** to the CPU/cache bus **31** when the value of register **37** becomes zero. Clearly, Park does not describe "logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus" as is recited in claim 19. Rather, Park describes the data as being continuously transmitted regardless of the status of the CPU/cache bus **31**. Additionally, Park does not employ a bus grant indication or any other form of indication as to whether or not the bus is available for transfer.

To establish a *prima facie* case of obviousness, the prior art must cited must teach or suggest all the claim limitations. Neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

For the reasons cited above, Applicants believe that independent claim 1 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 2-8 are dependent upon claim 1, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that independent claim 9 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 10-18 are dependent upon claim 9, and are therefore allowable as a matter of law.

For the reasons cited above, Applicants believe that independent claim 19 is patentable over Applicants' Admitted Prior Art in view of Park et al. and is believed to be in condition for allowance.

Claims 20-24 are dependent upon claim 19, and are therefore allowable as a matter of law.

For these reasons this application is now considered to be in condition for allowance and such action is earnestly solicited. If the Office is not fully persuaded as to the merits of Applicant's position, or if an Examiner's Amendment would place the pending claims in condition for allowance, a telephone call to the undersigned is requested.

Respectfully Submitted,

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Date

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